Applicant	Beasom	**COMMUNICATION REGARDING CERTIFICATE OF CORRECTION**
Patent No.	6,902,967	
Issue Date	6/7/2005	
Serial No.	10/811,360	
Attorney Docket No.	125.008US02	
Title: INTEGRATED CIRCUIT WITH A MOS STRUCTURE HAVING REDUCED PARASITE BIPOLAR TRANSISTOR ACTION		

ATTN: Certificate of Corrections Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicant hereby requests issuance of a Certificate of Correction in U.S. Letters Patent No. 6,902,967 as specified on the attached Certificate (Form PTO/SB/44). Please find enclosed documentation supporting errors identified in the above noted patent, referred to herein as Exhibits A and B.

With respect to the errors identified in the claims of the issued patent, Exhibit A is a copy of pages 1 to 11 of an Amendment and Response (including claims 1 to 55 as allowed) and a signed Certificate of Transmission indicating filing of the Response with the U.S. Patent & Trademark Office on November 26, 2004. Exhibit B is a copy of Cols. 13 to 18 of the issued patent. The identified errors constitute typographical errors and as such, do not introduce new matter.

Applicant believes these corrections as specified are necessary due to Office errors and does not believe that any fee is due for requesting a Certificate of Correction for this patent. However, if deemed necessary, the Office is authorized to charge any additional fees found due to Deposit Account No. 502432. Please contact the undersigned if you have any questions.

Respectfully submitted,

Date: December 14, 2007

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Enclosures

switch terminal S0' has a positive voltage that is more positive that the voltage on switch terminal **S0**, the drain junction of lateral NDMOS device **504** blocks the applied voltage.

Turn off of the solid state relay **500** is initialized when the LED is turned off. An output current of the photo diode stack **506** then goes to 0V. The turn off and gate protection circuit **508**, which in its simplest form may comprise a relatively large resistor, discharges the gate capacitance of gate G of the lateral NDMOS devices **502** and **504** thereby taking the gate source voltage back to 0V on both lateral NDMOS devices **502** and **504**.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement, which is calculated to achieve the same purpose, may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.

What is claimed is:

1. A method of forming a MOS device in an integrated circuit, the method comprising:

forming a body region in a substrate adjacent a surface of the substrate;

forming a source in the body region; and

forming a layer of narrow band gap material adjacent the surface of the substrate, the layer of narrow band gap material having a band gap narrower than a band gap of the substrate material, wherein at least a portion of the source is within the layer of narrow band gap material.

2. The method of claim **1**, wherein the narrow band gap material reduces parasitic transistor action.

3. The method of claim **1** , wherein the substrate is of a first conductivity type with a low doping density, the body region is of the first conductivity type and the source is of a second conductivity type with a high doping density.

4. The method of claim **1**, further comprising:

forming a layer of gate dielectric on the surface of the substrate;

depositing a layer gate material on the surface of the gate dielectric; and

patterning the layer of gate material to form a gate.

5. The method of claim **1**, wherein the source is formed deeper from the surface of the substrate than the layer of narrow band gap material.

6. The method of claim **1**, wherein the layer of narrow band gap material is formed by epitaxial growth.

7. The method of claim **1** , wherein the layer of narrow band gap material is made of GeSi.

8. The method of claim **1**, wherein the layer of narrow band gap material is formed by ion implant.

9. The method of claim **8**, wherein Ge ions are implanted to form the layer of narrow band gap material.

10. The method of claim **8**, further comprising:

forming a gate on the surface of the substrate; and

using a tilt angle implant technique to implant ions into the surface of the substrate and under a portion of a gate.

11. A method of forming a quasi-vertical DMOS for an integrated circuit, the method comprising;

forming a patterned first dielectric layer on the surface of a substrate, wherein a first portion of the surface of the substrate is exposed by the pattern;

forming a layer of narrow band gap material on the exposed first portion of the surface of the substrate, wherein the layer of narrow band gap material has a band gap that is narrower than the band gap of the substrate;

forming a second dielectric layer on the narrow band gap material;

depositing a gate proximate a medial portion of the second dielectric layer;

forming a pair of perimeter body regions in the substrate; wherein the gate is positioned between the perimeter body regions; and

forming a source in each body region, wherein at least apportion of the source is also formed in the layer of narrow band gap material.

12. The method of claim **11**, further comprising:

using the gate as a mask in forming the body regions to self-align the body regions with the gate; and

using the gate as mask in forming the sources to self-align the sources with the gate.

13. The method of claim **11**, wherein the forming of the body regions further comprise:

implanting dopants of a first conductivity type in the substrate; and

diffusing the dopants.

14. The method of claim **11**, further comprising:

forming body contact regions in each body region.

15. The method of claim **11**, wherein forming the body contact region; in each body region further comprise:

implanting a high concentration of dopants of the first conductivity type.

16. The method of claim **11**, further comprising;

forming a stop region of the first conductivity type in the substrate having a low doping density for each perimeter body region;

implanting the first conductivity type dopants in the substrate using the gate as a mask; and

diffusing the first conductivity dopants to form the body regions, wherein a first edge of each perimeter body region is defined by an associated edge of the gate end a second edge of each perimeter body region terminates in an associated stop region.

17. The method of claim **11**, further comprising:

forming a source-body contact adjacent on the surface of the substrate adjacent each source and each body to couple the sources to the body regions.

18. The method of claim **11**, wherein the first dielectric layer is formed by local oxidation (LOCOS).

19. The method of claim **11**, further comprising:

forming a buried layer of a second conductivity type with high doping density in the substrate, wherein the substrate is of a first conductivity type with a low doping density;

forming a epi layer of the second conductivity type with a low doping density in the substrate after the buried layer has been formed; and

forming a sinker region of the second conductivity type with a high doping density that extends from the surface of the substrate to the buried layer.

20. The method of claim **19**, further comprising:

removing a portion of the first dielectric layer to form a second exposed portion of the surface of the substrate adjacent the sinker region.

21. The method of claim **20**, further comprising:

forming a sinker-drain contact over the second exposed portion.

22. A method of forming a quasi-vertical DMOS for an integrated circuit, the method comprising:

forming patterned first dielectric layer on a surface of a substrate having a first portion of the surface of the substrate exposed by the pattern;

forming a layer of gate dielectric on the exposed first portion of the surface of the substrate;

depositing a gate proximate a medial portion of the layer of gate dielectric;

forming a pair of perimeter body regions in the substrate, wherein the gate is positioned between the perimeter body regions;

forming layers of narrow band gap material in portions of the body regions, wherein the layers of narrow band gap material have a narrower band gap than the band gap of the remaining portions of the body regions; and

forming a source in each body region, wherein at least apportion of the source is also formed in the layer of narrow band gap material.

23. The method of claim 22, further comprising:

using the gate as a mask in forming the body regions to self-align the body regions with the gate; and

using the gate as mask in forming the sources to self align the sources with the gate.

24. The method of claim 22, wherein the forming of the body regions further comprise;

implanting dopants of a first conductivity type in the substrate; and

diffusing the dopants.

25. The method of claim 22, further comprising:

forming body contact regions in each body region.

26. The method of claim 25, wherein forming the body contact regions in each body region further comprise:

implanting a high concentration of dopants of the first conductivity type.

27. The method of claim 22, further comprising;

forming a stop region of the first conductivity type in the substrate having a low doping density for each perimeter body region;

implanting the first conductivity type dopants in the substrate using the gate as a mask; and

diffusing the first conductivity dopants to form the perimeter body regions, wherein a first edge of each perimeter body region is defined by an associated edge of the gate and a second edge of each perimeter body region terminates in an associated stop region.

28. The method of claim 22, further comprising:

forming a source-body contact adjacent on the surface of the substrate adjacent each source and each body to couple the sources to the body regions.

29. The method of claim 22, further comprising:

forming a buried layer of a second conductivity type with high doping density in the substrate, wherein the substrate is of a first conductivity type with a low doping density;

forming a epi layer of the second conductivity type with a low doping density in the substrate after the buried layer has been formed, wherein the buried layer is positioned between the epi layer and a portion of the substrate having the first conductivity type with low doping density; and

forming a sinker region of the second conductivity type with a high doping density that extends from the surface of the substrate to the buried layer.

30. The method of claim 22, wherein the layers of narrow band gap material are formed by selected epi growth.

31. The method of claim 22, further comprising:

forming a isolation area to isolate the quasi-vertical DMOS from other devices in the integrated circuit.

32. The method of claim 22, wherein the layers of narrow band gap material are formed by ion implant.

33. The method of claim 32, further comprising:

using a tilt angle implant technique to allow the ions to extend under the gate.

34. The method of claim 32, further comprising:

using the gate and the first dielectric layer as a mask when implanting the ions to form the layer of narrow band gap material.

35. The method of claim 32, wherein Ge ions are used to form the layer of narrow band gap material.

36. The method of claim 32, further comprising:

using a photo resist mask when implanting the ions to form the layer of narrow band gap material.

37. The method of claim 36, further comprising:

using the photo resist mask to form the source regions.

38. A method of forming a lateral DMOS for an integrated circuit, the method comprising:

forming a body of a first conductivity type in a substrate of a first conductivity type with a low doping density, wherein the body is positioned adjacent a surface of the substrate;

forming a layer of narrow band gap material on the surface of the substrate adjacent the body, wherein the layer of narrow band gap material has a band gap that is narrower than the band gap of the body; and

forming a source of a second conductivity type with a high doping density in the body, wherein at least a portion of the source is farmed in the layer of narrow band gap material, further wherein the narrow band gap material suppresses carrier injection from the source into the body thereby reducing parasitic HFE.

39. The method of claim 38, further comprising:

forming a gate on a gate dielectric on the surface of the substrate before the body and source are formed; and

using the gate as a partial mask to self-align the body and the source.

40. The method of claim 38, further comprising:

using a source mask to form the source by ion implant; and

using the source mask to form the layer of narrow band gap material by ion implant.

41. The method of claim 38, further comprising:

forming the layer of narrow band gap material by ion implant.

42. The method of claim 38, further comprising:

forming the layer of narrow band gap material by tilt angle ion implant.

43. The method of claim 38, further comprising:

forming the layer of narrow band gap material by Ge implant.

44. The method of claim 38, further comprising:

forming the layer of narrow band gap material by selective epi.

45. The method of claim 38, wherein layer of narrow band gap material is formed before a gate is deposited.

46. The method of claim 38, further comprising:

forming a drain contact of the second conductivity type with a high doping density in the substrate adjacent the

surface of the substrate, wherein the drain contact is spaced a predetermined distance from the source.

47. The method of claim **46**, further comprising:

forming a drain extension of the second conductivity type adjacent the surface of the substrate, wherein the dram extension extends from proximate the gate to the drain contact.

48. The method of claim **38**, wherein the lateral DMOS is formed in an isolation island in the integrated circuit, a method of forming the isolation island comprising:

covering an handle wafer with an isolation dielectric layer;

bonding a device wafer to the handle wafer;

patterning the device wafer to form isolation trenches; and

forming an isolation dielectric layer on side walls of the isolation trenches.

49. The method of claim **48**, further comprising:

filling the trench regions with poly silicon.

50. A method of forming a vertical DMOS comprising:

forming a drain region in a substrate of a first conductivity type with a low dopant density;

forming a body region in the substrate of a second conductivity type over the drain region;

forming a layer of narrow band gap material in the substrate, wherein the layer of narrow band gap material has a narrower band gap than portions of the body region;

forming at least one source region of the first conductivity type with high dopant density in the body, wherein at least a portion of each source region is formed in the layer of narrow band gap material; and

forming at least one gate.

51. The method of claim **50**, wherein forming each gate further comprises:

etching the substrate to form a trench for each gate;

depositing a layer of dielectric to coat interior surfaces of each trench; and

depositing each gate in an associated trench.

52. The method of claim **50**, wherein the layer of narrow band gap material is formed by epitaxial growth.

53. The method of claim **50**, wherein forming the layer of narrow band gap further comprises:

implanting ions.

54. The method of claim **50**, wherein each body region is formed deeper from the working surface of the substrate than the layer of narrow band gap material.

55. The method of claim **50**, wherein the source region is formed deeper from the working surface of the substrate than the layer of narrow band gap material.

* * * * *

Applicant(s)	Beasom	**AMENDMENT AND RESPONSE UNDER 37 C.F.R. § 1.111**
Serial No.	10/811,360	
Filing Date	3/26/2004	
Group Art Unit	2825	
Examiner Name	Chuong A. Luu	
Confirmation No.	2091	
Attorney Docket No.	125.008US02	
Title: INTEGRATED CIRCUIT WITH A MOS STRUCTURE HAVING REDUCED PARASITE BIPOLAR TRANSISTOR ACTION		

Commissioner for Patents
P.O. Box 1450
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Applicants have reviewed the Office Action mailed on August 25, 2004. Please enter the following response to the above-identified application as follows.

The Claims are reflected in the listing of claims that begins on page 2 of this paper.

Remarks begin on page 12 of this paper.

Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of claims:

1. (Original) A method of forming a MOS device in an integrated circuit, the method comprising:

forming a body region in a substrate adjacent a surface of the substrate;

forming a source in the body region; and

forming a layer of narrow band gap material adjacent the surface of the substrate, the layer of narrow band gap material having a band gap narrower than a band gap of the substrate material, wherein at least a portion of the source is within the layer of narrow band gap material.

2. (Original) The method of claim 1, wherein the narrow band gap material reduces parasitic transistor action.

3. (Original) The method of claim 1, wherein the substrate is of a first conductivity type with a low doping density, the body region is of the first conductivity type and the source is of a second conductivity type with a high doping density.

4. (Original) The method of claim 1, further comprising:
forming a layer of gate dielectric on the surface of the substrate;
depositing a layer gate material on the surface of the gate dielectric; and
patterning the layer of gate material to form a gate.

5. (Original) The method of claim 1, wherein the source is formed deeper from the surface of the substrate than the layer of narrow band gap material.

6. (Original) The method of claim 1, wherein the layer of narrow band gap material is formed by epitaxial growth.

7. (Original) The method of claim 1, wherein the layer of narrow band gap material is made of GeSi.

8. (Original)The method of claim 1, wherein the layer of narrow band gap material is formed by ion implant.

9. (Original) The method of claim 8, wherein Ge ions are implanted to form the layer of narrow band gap material.

10. (Original) The method of claim 8, further comprising:

forming a gate on the surface of the substrate; and

using a tilt angle implant technique to implant ions into the surface of the substrate and under a portion of a gate.

11. (Original) A method of forming a quasi-vertical DMOS for an integrated circuit, the method comprising:

forming a patterned first dielectric layer on the surface of a substrate, wherein a first portion of the surface of the substrate is exposed by the pattern;

forming a layer of narrow band gap material on the exposed first portion of the surface of the substrate, wherein the layer of narrow band gap material has a band gap that is narrower than the band gap of the substrate;

forming a second dielectric layer on the narrow band gap material;

depositing a gate proximate a medial portion of the second dielectric layer;

forming a pair of perimeter body regions in the substrate, wherein the gate is positioned between the perimeter body regions; and

forming a source in each body region, wherein at least apportion of the source is also formed in the layer of narrow band gap material.

12. (Original) The method of claim 11, further comprising:

using the gate as a mask in forming the body regions to self-align the body regions with the gate; and

using the gate as mask in forming the sources to self-align the sources with the gate.

13. (Original) The method of claim 11, wherein the forming of the body regions further comprise:

implanting dopants of a first conductivity type in the substrate; and

diffusing the dopants.

14. (Original) The method of claim 11, further comprising:

forming body contact regions in each body region.

15. (Original) The method of claim 11, wherein forming the body contact regions in each body region further comprise:

implanting a high concentration of dopants of the first conductivity type.

16. (Original) The method of claim 11, further comprising;

forming a stop region of the first conductivity type in the substrate having a low doping density for each perimeter body region;

implanting the first conductivity type dopants in the substrate using the gate as a mask; and

diffusing the first conductivity dopants to form the body regions, wherein a first edge of each perimeter body region is defined by an associated edge of the gate and a second edge of each perimeter body region terminates in an associated stop region.

17. (Original) The method of claim 11, further comprising:

forming a source–body contact adjacent on the surface of the substrate adjacent each source and each body to couple the sources to the body regions.

18. (Original) The method of claim 11 wherein the first dielectric layer is formed by local oxidation (LOCOS).

19. (Original) The method of claim 11, further comprising:

forming a buried layer of a second conductivity type with high doping density in the substrate, wherein the substrate is of a first conductivity type with a low doping density;

forming a epi layer of the second conductivity type with a low doping density in the substrate after the buried layer has been formed; and

forming a sinker region of the second conductivity type with a high doping density that extends from the surface of the substrate to the buried layer.

20. (Original) The method of clam 19, further comprising:

removing a portion of the first dielectric layer to form a second exposed portion of the surface of the substrate adjacent the sinker region.

21. (Original) The method of claim 20, further comprising:

forming a sinker-drain contact over the second exposed portion.

22. (Original) A method of forming a quasi-vertical DMOS for an integrated circuit, the method comprising:

forming patterned first dielectric layer on a surface of a substrate having a first portion of the surface of the substrate exposed by the pattern;

forming a layer of gate dielectric on the exposed first portion of the surface of the substrate;

depositing a gate proximate a medial portion of the layer of gate dielectric;

forming a pair of perimeter body regions in the substrate, wherein the gate is positioned between the perimeter body regions;

forming layers of narrow band gap material in portions of the body regions, wherein the layers of narrow band gap material have a narrower band gap than the band gap of the remaining portions of the body regions; and

forming a source in each body region, wherein at least apportion of the source is also formed in the layer of narrow band gap material.

23. (Original) The method of claim 22, further comprising:

using the gate as a mask in forming the body regions to self-align the body regions with the gate; and

using the gate as mask in forming the sources to self align the sources with the gate.

24. (Original) The method of claim 22, wherein the forming of the body regions further comprise:

implanting dopants of a first conductivity type in the substrate; and

diffusing the dopants.

25. (Original) The method of claim 22, further comprising:

forming body contact regions in each body region.

26. (Original) The method of claim 25, wherein forming the body contact regions in each body region further comprise:

implanting a high concentration of dopants of the first conductivity type.

27. (Original) The method of claim 22, further comprising;

forming a stop region of the first conductivity type in the substrate having a low doping density for each perimeter body region;

implanting the first conductivity type dopants in the substrate using the gate as a mask; and

diffusing the first conductivity dopants to form the perimeter body regions, wherein a first edge of each perimeter body region is defined by an associated edge of the gate and a second edge of each perimeter body region terminates in an associated stop region.

28. (Original) The method of claim 22, further comprising:

forming a source–body contact adjacent on the surface of the substrate adjacent each source and each body to couple the sources to the body regions.

29. (Original) The method of claim 22, further comprising:

forming a buried layer of a second conductivity type with high doping density in the substrate, wherein the substrate is of a first conductivity type with a low doping density;

forming a epi layer of the second conductivity type with a low doping density in the substrate after the buried layer has been formed, wherein the buried layer is positioned between the epi layer and a portion of the substrate having the first conductivity type with low doping density; and

forming a sinker region of the second conductivity type with a high doping density that extends from the surface of the substrate to the buried layer.

30. (Original) The method of claim 22, wherein the layers of narrow band gap material are formed by selected epi growth.

31. (Original) The method of claim 22, further comprising:

forming a isolation area to isolate the quasi-vertical DMOS from other devices in the integrated circuit.

32. (Original) The method of claim 22, wherein the layers of narrow band gap material are formed by ion implant.

33. (Original) The method of claim 32, further comprising:

using a tilt angle implant technique to allow the ions to extend under the gate.

34. (Original) The method of claim 32, further comprising:

using the gate and the first dielectric layer as a mask when implanting the ions to form the layer of narrow band gap material.

35. (Original) The method of claim 32, wherein Ge ions are used to form the layer of narrow band gap material.

36. (Original) The method of claim 32, further comprising:

using a photo resist mask when implanting the ions to form the layer of narrow band gap material.

37. (Original) The method of claim 36, further comprising:

using the photo resist mask to form the source regions.

38. (Original) A method of forming a lateral DMOS for an integrated circuit, the method comprising:

forming a body of a first conductivity type in a substrate of a first conductivity type with a low doping density, wherein the body is positioned adjacent a surface of the substrate;

forming a layer of narrow band gap material on the surface of the substrate adjacent the body, wherein the layer of narrow band gap material has a band gap that is narrower than the band gap of the body; and

forming a source of a second conductivity type with a high doping density in the body, wherein at least a portion of the source is formed in the layer of narrow band gap material, further wherein the narrow band gap material suppresses carrier injection from the source into the body thereby reducing parasitic HFE.

39. (Original) The method of claim 38, further comprising:

forming a gate on a gate dielectric on the surface of the substrate before the body and source are formed; and

using the gate as a partial mask to self-align the body and the source.

40. (Original) The method of claim 38, further comprising:

using a source mask to form the source by ion implant; and

using the source mask to form the layer of narrow band gap material by ion implant.

41. (Original) The method of claim 38, further comprising:

forming the layer of narrow band gap material by ion implant.

42. (Original) The method of claim 38, further comprising:

forming the layer of narrow band gap material by tilt angle ion implant.

43. (Original) The method of claim 38, further comprising:

forming the layer of narrow band gap material by Ge implant.

44. (Original) The method of claim 38, further comprising:

forming the layer of narrow band gap material by selective epi.

45. (Original) The method of claim 38, wherein layer of narrow band gap material is formed before a gate is deposited.

46. (Original) The method of claim 38, further comprising:

forming a drain contact of the second conductivity type with a high doping density in the substrate adjacent the surface of the substrate, wherein the drain contact is spaced a predetermined distance from the source.

47. (Original) The method of claim 46, further comprising:

forming a drain extension of the second conductivity type adjacent the surface of the substrate, wherein the drain extension extends from proximate the gate to the drain contact.

48. (Original) The method of claim 38, wherein the lateral DMOS is formed in an isolation island in the integrated circuit, a method of forming the isolation island comprising:

covering an handle wafer with an isolation dielectric layer;

bonding a device wafer to the handle wafer;

patterning the device wafer to form isolation trenches; and

forming an isolation dielectric layer on side walls of the isolation trenches.

49. (Original) The method of claim 48, further comprising:

filling the trench regions with poly silicon.

50. (Original) A method of forming a vertical DMOS comprising:

forming a drain region in a substrate of a first conductivity type with a low dopant density;

forming a body region in the substrate of a second conductivity type over the drain region;

forming a layer of narrow band gap material in the substrate, wherein the layer of narrow band gap material has a narrower band gap than portions of the body region;

forming at least one source region of the first conductivity type with high dopant density in the body, wherein at least a portion of each source region is formed in the layer of narrow band gap material; and

forming at least one gate.

51. (Original) The method of claim 50, wherein forming each gate further comprises:

etching the substrate to form a trench for each gate;

depositing a layer of dielectric to coat interior surfaces of each trench; and

depositing each gate in an associated trench.

52. (Original) The method of claim 50, wherein the layer of narrow band gap material is formed by epitaxial growth.

53. (Original) The method of claim 50, wherein forming the layer of narrow band gap further comprises:

implanting ions.

54. (Original) The method of claim 50, wherein each body region is formed deeper from the working surface of the substrate than the layer of narrow band gap material.

55. (Original) The method of claim 50, wherein the source region is formed deeper from the working surface of the substrate than the layer of narrow band gap material.

EXHIBIT A

Applicant(s)	James D.Beasom	**FACSIMILE TRANSMITTAL FORM**
Serial No.	10/811,360	
Filing Date	Mar 26, 2004	
Group Art Unit	2825	
Examiner Name	Chuong A Luu	
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TOTAL PAGES: 17 pgs. (including cover sheet)
TO CENTRAL FAX – (703) 872-9306
Attention: Examiner Chuong A Luu , Art Unit 2825

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Enclosures

The following documents are enclosed:

X An Amendment and Response Under 37 C.F.R. 1.111 (16 pgs.).

Please charge any additional fees or credit any overpayments to Deposit Account No. 502432.

Submitted By

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Signature				Date	November 26, 2004

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Certificate of Transmission

I certify that this paper, and the above-identified documents, are being transmitted by facsimile to, Examiner Chuong A Luu, Group Art Unit 2825 (Facsimile No. 703-872-9306) of the United States Patent and Trademark Office on November 26, 2004.

Name	Scott V. Lundberg	Signature	